Amendments to the Specification:

Please replace paragraph beginning on page 14, line 12 with the following amended paragraph:

FIGS. 2A-2E depict significant waveforms that arise at various stages in tuning apparatus 10 during the course of a tuning process. As may be seen from FIG. 2A, at T_0, a transition in CLK 140, from low to high, precipitates the tuning process. As CLK 140 goes to a logic ONE, NO switching device 112a closes, and NC switching device 112b opens, thereby respectively connecting capacitance 113 to transconductance 111 and coupling node 114 to (-) input 131a of comparator 130. In one embodiment, concurrent with the reorientation of switching devices 112a and 112b, CLK 140 may operate to enable comparator [[140]] 130 and CLK 160, and to reset sampler 150. In this sense, then, CLK 160 may be viewed as synchronization clock, in that it provides a signal that synchronizes components invoked in the tuning process.

Please replace paragraph beginning on page 20, line 20 with the following amended paragraph:

In addition, skilled practioners undoubtedly discern the design assumption that is implicit in the above-described embodiment. Specifically, in one embodiment, in order to foreclose the possibility of ambiguity in the sampler output, then the achievable tolerance in tuning capacitance 113 must be such that the charging period of Gm-C time-constant circuit 110, will, for all values of transconductance 111 and capacitance 113, be equal to $T_s \pm \Delta T_s$, where T_s is the nominal period of CLK 160, and Δ is a fraction less than, for example, ½. Alternatively, if prevailing process tolerances are such that the above assumption is not justified, then additional logic may be indicated. In one implementation, the logic may operate to detect a particular transition in the output of CLK 160. If that transition occurs while the output of comparator 130 remains a logic ONE, then the tuning error signal (output 154 of sampler 150) will be ~~clamed~~ clamped to a logic ZERO, for example. In particular, with regard to the implementation described herein above, if output 133 persists at a logic ONE upon the second rising edge in CLK 160, then output 150 will be forced to a logic ZERO.